Migrating from AT89S8252/S53 to AT89S8253

New Features

- **64-byte User Signature Array**
- **Enhanced UART with Frame Detection and Automatic Address Recognition**
- **Enhanced SPI (Double Write/Read Buffered) Serial Interface**
- **Page Mode in both Parallel/Serial Programming Modes (Code/Data Memories)**
- **Four-level Enhanced Interrupt Controller**
- **Programmable and Fuseable x2 Clock Option**
- **Internal Power-on Reset**
- **42-pin PDIP Package Option for Reduced EMI Emission**
- **EEPROM Page Write Access during CPU Execution**

1. Introduction

The purpose of this application note is to help users convert existing designs from AT89S8252/S53 to AT89S8253. The given information will also help migration from AT89LS8252/LS53 to AT89S8253. This application note describes AT89S8253 memory sizes, features, and SFR mapping. More detailed information can be found in the AT89S8253 datasheet.

2. Memory Sizes

The following table shows a comparison of the individual memories.

Memory	AT89S8252	AT89S53	AT89S8253
Flash	8K Bytes	12K Bytes	12K Bytes
RAM	256 Bytes	256 Bytes	256 Bytes
EEPROM	2K Bytes	N/A	2K Bytes

3. 64-byte User Signature Array

Sixty-four bytes are accessible to the user to program their own desired data. Bytes can be either programmed by parallel or serial mode.

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4. Enhanced UART with Frame Error Detection and Automatic Address Recognition

When used for frame error detection, the UART looks for missing stop bits in the communication. A missing bit will set the FE bit in the SCON Register. Automatic Address Recognition allows the UART to recognize certain addresses in the serial bit stream by using hardware to make the comparison.

5. Enhanced SPI (Double Write/Read Buffered) Serial Interface

The enhanced SPI mode allows the write buffer to hold the next byte to be transmitted. As long as the CPU can keep the write buffer full, multiple bytes may be transferred with minimal latency between bytes.

6. Page Mode in both Parallel/Serial Programming Modes (Code/Data Memories)

Program and data memories can be programmed in page mode (1 code page = 64 bytes; data page = 32 bytes).

Page mode is available in both the parallel and serial programming modes.

7. Four-level Enhanced Interrupt Controller

Each interrupt source can be individually programmed to one of four priority levels by setting or clearing a bit in the Interrupt Priority (IP) register and in the Interrupt Priority High (IPH) register.

The Interrupt Priority High register shows the bit values and priority levels associated with each combination.

8. Programmable and Fuseable x2 Clock Option

The x2 clock option allows the microcontroller to execute one machine cycle in 6 clock periods instead of 12 clock periods. This can be set either through hardware or software.

9. Internal Power-On Reset

A 1 ms internal reset signal will be generated after power-on, eliminating the need for any external Power-on reset circuitry.

10. 42-pin PDIP Package Option for Reduced EMI Emission

The 42-pin package has extra pins PWRVDD and PWRGND to reduce EMI Emission. PWRVDD must be connected to the application board supply voltage. PWRGND must be connected to the application board GND.

11. EEPROM Page Write during CPU Execution

During CPU execution, EEPROM can be written one page (32 bytes) at a time. This way, 32 bytes will only require 4 ms of programming time instead of 128 ms required in single byte programming. During program execution mode (using the MOVX instruction) there is an auto-erase capability at the byte level. This is useful, for example, when the user wants to update or modify a single EEPROM byte location in real-time without affecting any other bytes.

12. Operational V_{CC} Voltage Range

While the AT89S8252/S53 are offered in low-voltage versions as AT89LS8252/LS53, respectively, the AT89S8253 nomenclature encompasses both the regular (4.0V to 5.5V) and low-voltage (2.7V to 4.0V) operational V_{CC} voltage ranges. The ordering is designated by the appropriate operational frequency range. Please consult the Ordering Information table in the AT89S8253 device datasheet.

13. Clock Loading

Due to its low power consumption capability, the internal clock design of the AT89S8253 has a different set of clock loading requirements. Refer to the device datasheet for the recommended C1, C2 load range.

14. SFRs Mapping

The highlighted SFR locations are new registers for the AT89S8253 device.

0F8H									0FFH
0F0H	B								0F7H
0E8H									0EFH
0E0H	ACC								0E7H
0D8H									0DFH
0D0H	PSW					SPCR			0D7H
0C8H	T2CON	T2MOD	RCAP2L	RCAP2H	TL2	TH2			0CFH
0C0H									0C7H
0B8H	IP	SADEN							0BFH
0B0H	P3							IPH	0B7H
0A8H	IE	SADDR	SPSR						0AFH
0A0H	P2						WDTRST	WDTCON	0A7H
98H	SCON	SBUF							9FH
90H	P1						EECON		97H
88H	TCON	TMOD	TL0	TL1	TH0	TH1	AUXR	CLKREG	8FH
80H	P0	SP	DP0L	DP0H	DP1L	DP1H	SPDR	PCON	87H

15. Fuse Table

Fuse	AT89S8252	AT89S53	AT89S8253
SerialProg	Yes	Yes	Yes
x2 Clock	No	No	Yes
UserRowProg	No	No	Yes

16. Programming Time (Byte Mode)

Part Number	Flash (Reset = High)	EEPROM (Reset = High)	EEPROM Reset = Low (CPU Execution)
AT89S8252	12 sec	2.7 sec	5.12 sec
AT89S53	16 sec	N/A	N/A
AT89S8253	N/A	N/A	N/A

17. Programming Time (Page Mode)

Part Number	Flash (Reset = High)	EEPROM (Reset = High)	EEPROM Reset = Low (CPU Execution)
AT89S8252	N/A	N/A	N/A
AT89S53	N/A	N/A	N/A
AT89S8253	0.96 sec	0.32 sec	0.256 sec

18. Parallel and Serial Mode Programming Differences

For serial programming, the AT89S8252/S53 uses a 3-byte serial protocol, while the AT89S8253 uses a 4-byte protocol. In addition, serial input on MOSI is sampled by SCK during its **negative** transition edge. Users of third-party programmers should download the AT89S8253 driver for their particular programmer.

In both parallel/serial programming modes, there is no auto-erase capability (unlike the AT89S8252/S53 devices) for either the Flash program or EEPROM data memory. If the user needs to reprogram any location which had been previously programmed, a Chip Erase operation is required.

For parallel programming, the AT89S8252/S53 uses P2.6, P2.7, P3.6, and P3.7 as control signals for parallel mode programming. Users should be aware that the AT89S8253 uses P3.3, P3.4, P3.5, P3.6, and P3.7 as control signals for parallel mode programming.

18.1 RDY/$\overline{\text{BSY}}$ Differences

18.1.1 Program Flash

The AT89S8252/S53 uses P3.4 as a RDY/$\overline{\text{BSY}}$ pin to indicate the progress of byte programming in the parallel programming mode.

The AT89S8253 uses P3.0 as a RDY/$\overline{\text{BSY}}$ pin to indicate the progress of byte programming in the parallel programming mode.

18.2 EEPROM Differences

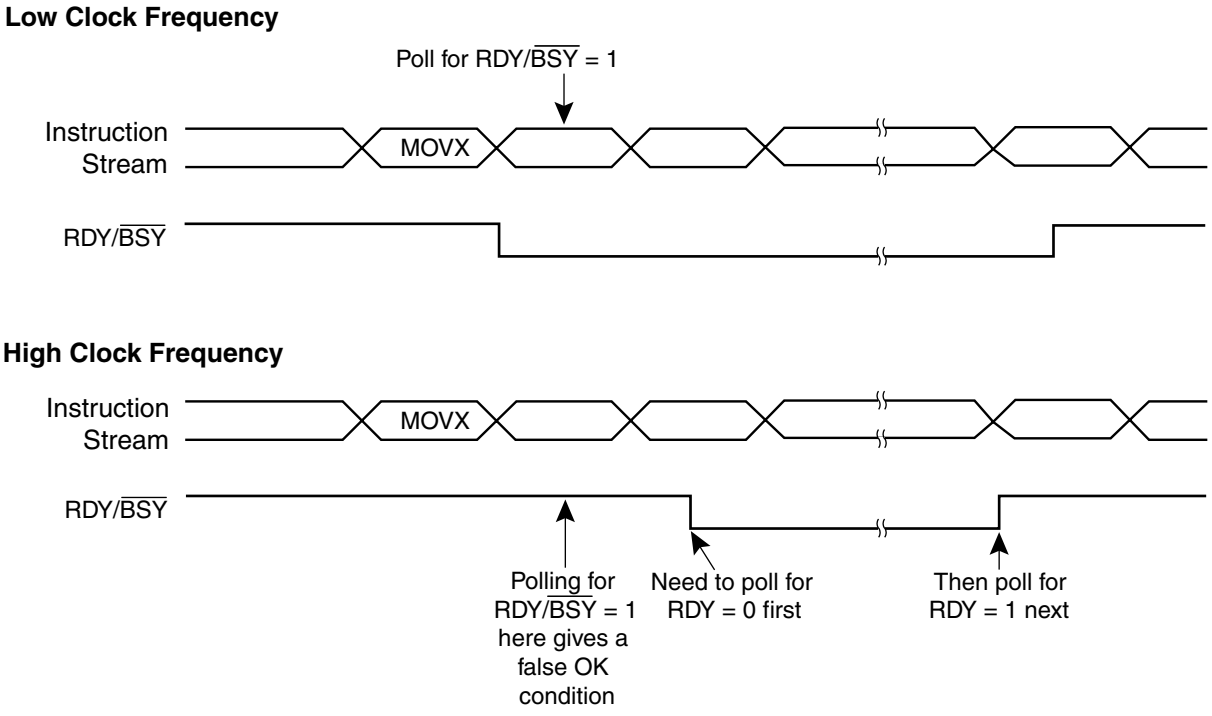
Below is sample code that writes one page of data to EEPROM:

```
EEMWE  EQU  00010000B     ;EEPROM data memory write enable
EEMEN  EQU  00001000B     ;internal EEPROM access enable
EELD   EQU  00100000B     ;EEPROM memory load enable bit

ORL    EECON,#EEMEN       ;enable EEPROM accesses
ORL    EECON,#EEMWE       ;enable EEPROM writes
ORL    EECON,#EELD        ;enable EEPROM page load
MOV    R7,#1FH            ;0x1FH = 31
PAGELOAD:
MOV    A,#055H            ;byte loaded into Accumulator
MOVX   @DPTR,A            ;Load byte to data buffer
INC    DPTR               ;increment DPTR(EEPROM address)
DJNZ   R7,PAGELOAD        ;check if 31 bytes have been loaded

;LOAD LAST BYTE AND INITIATE PAGE WRITE

MOV    A,#055H            ;byte loaded into Accumulator
XRL    EECON,#EELD        ;the next will MOVX will start the write cycle
MOVX   @DPTR,A            ;Load byte to data buffer
```

At higher frequencies (i.e. F ≥ 16 MHz), if polling the RDY/$\overline{\text{BSY}}$ bit during AT89S8253 EEPROM writes, it becomes necessary to poll for both the start and the end of the EEPROM write cycle. The sample code below illustrates this (see Figure 18-1 on page 6):

```
WRITESTART:               ;Wait for write cycle to start (RDY/BSY=low)
MOV    VAR,096H           ;096H is the EECON SFR
JB     VAR.1,Writestart
WAIT:                     ;Wait until write cycle is finished
MOV    VAR,096H
JNB    VAR.1,Wait
```

Figure 18-1. Data EEPROM Polling Sequence



18.3 Register Differences

The following highlights register differences and their corresponding bits in the AT89S8252/S53 and AT89S8253.

AT89S8252			AT89S8253		
Register	**Address**		**Register**	**Address**	
WMCON	96H	PS2 PS1 PS0 EEMWE EEMEN DPS WDTRST WDTEN	EECON	96H	-- -- EELD EEMWE EEMEN DPS RDY/BSY WRTINH
			WDTCON	A7H	PS2 PS1 PS0 WDIDLE DISRTO HWDT WSWRST WDTEN
SPSR	AAH	SPIF WCOL -- -- -- -- --	SPSR	AAH	SPIF WCOL LDEN -- -- -- DISSO ENH

AT89S53			AT89S8253		
Register	**Address**		**Register**	**Address**	
WCON	96H	PS2 PS1 PS0 -- -- DPS WDTRST WDTEN	EECON	96H	-- -- EELD EEMWE EEMEN DPS RDY/BSY WRTINH
			WDTCON	A7H	PS2 PS1 PS0 WDIDLE DISRTO HWDT WSWRST WDTEN
SPSR	AAH	SPIF WCOL -- -- -- -- --	SPSR	AAH	SPIF WCOL LDEN -- -- -- DISSO ENH

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Atmel Corporation

2325 Orchard Parkway
San Jose, CA 95131, USA
Tel: 1(408) 441-0311
Fax: 1(408) 487-2600

Regional Headquarters

Europe
Atmel Sarl
Route des Arsenaux 41
Case Postale 80
CH-1705 Fribourg
Switzerland
Tel: (41) 26-426-5555
Fax: (41) 26-426-5500

Asia
Room 1219
Chinachem Golden Plaza
77 Mody Road Tsimshatsui
East Kowloon
Hong Kong
Tel: (852) 2721-9778
Fax: (852) 2722-1369

Japan
9F, Tonetsu Shinkawa Bldg.
1-24-8 Shinkawa
Chuo-ku, Tokyo 104-0033
Japan
Tel: (81) 3-3523-3551
Fax: (81) 3-3523-7581

Atmel Operations

Memory
2325 Orchard Parkway
San Jose, CA 95131, USA
Tel: 1(408) 441-0311
Fax: 1(408) 436-4314

Microcontrollers
2325 Orchard Parkway
San Jose, CA 95131, USA
Tel: 1(408) 441-0311
Fax: 1(408) 436-4314

La Chantrerie
BP 70602
44306 Nantes Cedex 3, France
Tel: (33) 2-40-18-18-18
Fax: (33) 2-40-18-19-60

ASIC/ASSP/Smart Cards
Zone Industrielle
13106 Rousset Cedex, France
Tel: (33) 4-42-53-60-00
Fax: (33) 4-42-53-60-01

1150 East Cheyenne Mtn. Blvd.
Colorado Springs, CO 80906, USA
Tel: 1(719) 576-3300
Fax: 1(719) 540-1759

Scottish Enterprise Technology Park
Maxwell Building
East Kilbride G75 0QR, Scotland
Tel: (44) 1355-803-000
Fax: (44) 1355-242-743

RF/Automotive
Theresienstrasse 2
Postfach 3535
74025 Heilbronn, Germany
Tel: (49) 71-31-67-0
Fax: (49) 71-31-67-2340

1150 East Cheyenne Mtn. Blvd.
Colorado Springs, CO 80906, USA
Tel: 1(719) 576-3300
Fax: 1(719) 540-1759

Biometrics/Imaging/Hi-Rel MPU/
High Speed Converters/RF Datacom
Avenue de Rochepleine
BP 123
38521 Saint-Egreve Cedex, France
Tel: (33) 4-76-58-30-00
Fax: (33) 4-76-58-34-80

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